Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus comprising:

an inductor having an impedance connected in series between an output of a high frequency circuit operating at a frequency and an electrostatic discharge (ESD) circuit configured to protect the high frequency circuit from an ESD event, the impedance having a substantially high value at that frequency and a substantially low value at the ESD event; and

an ESD clamp circuit to clamp a supply voltage at a predetermined level to provide protection from a voltage surge or a high current spike when the ESD event occurs.

2. (original) The apparatus of claim 1 wherein the ESD circuit has first and second terminals, the first terminal being connected to one end of the inductor, the second terminal being connected to ground.

3. (original) The apparatus of claim 1 wherein the ESD circuit is a gate grounded metal oxide semiconductor (NMOS) transistor.

4. (original) The apparatus of claim 1 wherein the ESD circuit is a diode circuit.

5. (original) The apparatus of claim 1 wherein the inductor is connected between a first bond pad of the output and a second bond pad of the ESD circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency circuit and the ESD circuit.

6. (original) The apparatus of claim 5 wherein the inductor is connected between the first and second bond pads via first and second bond wires.

7. (original) The apparatus of claim 5 wherein the high frequency and ESD circuits are on a silicon die mounted on the package substrate.

8. (original) The apparatus of claim 5 wherein the package is one of a ball grid array (BGA) package and a flip-chip package.

9. (original) The apparatus of claim 1 wherein the frequency is higher than 1 gigahertz.

10. (original) The apparatus of claim 1 wherein the ESD event corresponds to a low frequency event.

11. (currently amended) A method comprising:

connecting an inductor in series between an output of the high frequency circuit operating at a frequency and an electrostatic discharge (ESD) circuit configured to protect the high frequency circuit from an ESD event, the inductor having an impedance with a substantially high value at the frequency and a substantially low value at the ESD event; and

clamping a supply voltage at a predetermined level by an ESD clamp circuit to provide protection from a voltage surge or a high current spike when the ESD event occurs.

12. (original) The method of claim 11 wherein connecting the inductor comprises:

connecting a first terminal of the ESD circuit to one end of the inductor, and connecting a second terminal of the ESD circuit to ground.

13. (original) The method of claim 11 wherein the ESD circuit is a gate grounded metal oxide semiconductor (NMOS) transistor.

14. (original) The method of claim 11 wherein the ESD circuit is a diode circuit.

15. (original) The method of claim 11 wherein connecting the inductor comprises connecting the inductor between a first bond pad of the output and a second bond pad of the ESD

circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency circuit and the ESD circuit.

16. (original) The method of claim 15 wherein connecting the inductor comprises connecting one end of the inductor to the first bond pad via a first bond wire; and connecting an other end of the inductor to the second bond pad via a second bond wire.

17. (original) The method of claim 15 wherein connecting the inductor comprises:

mounting a silicon die containing the high frequency and ESD circuits on the package substrate.

18. (original) The method of claim 15 wherein the package is one of a ball grid array (BGA) package and a flip-chip package.

19. (original) The method of claim 11 wherein the frequency is higher than 1 gigahertz.

20. (original) The method of claim 11 wherein the ESD event corresponds to a low frequency event.

21. (currently amended) A circuit comprising:

a high frequency circuit operating at a frequency, the high frequency circuit having an output;

an electrostatic discharge (ESD) circuit configured to protect the high frequency circuit from an ESD event;

an ESD clamp circuit to clamp a supply voltage at a predetermined level to provide protection from a voltage surge or a high current spike when the ESD event occurs; and

an inductor having an impedance connected in series between the output of the high frequency circuit and the electrostatic discharge (ESD) circuit, the impedance having a substantially high value at the frequency and a substantially low value at the ESD event.

22. (original) The circuit of claim 11 wherein the ESD circuit has first and second terminals, the first terminal being connected to one end of the inductor, the second terminal being connected to ground.

23. (original) The circuit of claim 11 wherein the ESD circuit is a gate grounded metal oxide semiconductor (NMOS) transistor.

24. (original) The circuit of claim 11 wherein the ESD circuit is a diode circuit.

25. (original) The circuit of claim 11 wherein the inductor is connected between a first bond pad of the output and a second bond pad of the ESD circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency circuit and the ESD circuit.

26. (original) The circuit of claim 15 wherein the inductor is connected between the first and second bond pads via first and second bond wires.

27. (original) The circuit of claim 15 wherein the high frequency and ESD circuits are on a silicon die mounted on the package substrate.

28. (original) The circuit of claim 15 wherein the package is one of a ball grid array (BGA) package and a flip-chip package.

29. (original) The circuit of claim 11 wherein the frequency is higher than 1 gigahertz.

30. (original) The circuit of claim 11 wherein the ESD event corresponds to a low frequency event.